UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,034	11/01/2001	Alexander Saldanha	21891.02101	4992

7590 05/05/2005

Crosby, Heafey, Roach & May
P.O. Box 7936
San Francisco, CA 94120-7936

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/002,034	SALDANHA ET AL.
	Examiner	Art Unit
	Naum B. Levin	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/002,034 and amendment filed on 02/15/2005. Claims 1-23 remain pending in the application. Based on the Applicant's remarks Examiner has performed additional search, and found a new reference.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 8-9, 13-14 and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dupenloup (US Patent 6,205,572).

As to claims 1, 8, 13 and 17 Dupenloup discloses:

(1), (17) A method/computer readable media having stored instructions for synthesizing an integrated circuit design, the method comprising (col.78, ll.9-18):

performing physical optimization (improvement to minimize layout area) of block (module) and wire placement, before performing logic synthesis (col.79, ll.33-67; col.80, ll.1-25);

partitioning (dissolving/pure down) the blocks (modules) into cores (sub-modules) and shells (combinational logic/output "registered", or driven, by flipflop) (col.10, ll.8-22; col.15, ll.20-47);

synthesizing (creating/grouping/ungrouping) the shells and cores (col.15, ll.58-67; col.45, ll.31-53; col.47, ll.26-38); and

recombining (re-arranging) the cores and shells into blocks (loop for physical optimization) (col.45, ll.31-38; col.45, ll.54-67; col.46, ll.1-32);

(8) A method for designing integrated circuits, the method comprising:

performing layout of physical blocks (modules) by estimating an area for each block (col.79, ll.50-62);

connecting pins of the blocks (modules) with no timing constraints ("In global routing, connections are completed between the proper blocks of the circuit disregarding the exact geometric details of each wire and terminal.") (col.79, ll.63-67; col.80, ll.1-11);

assigning each wire to a metal layer pair (col.80, ll.12-17);

optimizing the speed (delay/timing) of each wire for its respective layer (col.41, ll.11-28; col.70, ll.45-52; col.80, ll.12-17);

partitioning (dissolving/pure down) the blocks (modules) into cores (sub-modules) and shells (combinational logic/output "registered", or driven, by flipflop) (col.10, ll.8-22; col.15, ll.20-47);

synthesizing (creating/grouping/ungrouping) the shells (col.15, ll.58-67; col.45, ll.31-53; col.47, ll.26-38);

synthesizing the cores (col.15, ll.58-67; col.45, ll.31-53; col.47, ll.26-38); and

recombining (re-arranging) the cores and shells into blocks (loop for physical optimization) (col.45, ll.31-38; col.45, ll.54-67; col.46, ll.1-32);

(13) A method for reducing design cycle time for integrated circuits, the method comprising:

laying out blocks (modules) by estimating an area for each block col.79, ll.63-67; col.80, ll.1-11);

minimizing a delay in each global wire (col.41, ll.11-28; col.70, ll.45-52; col.80, ll.12-17);

partitioning (dissolving/pure down) each block (module) into a core (sub-module) and shells (combinational logic/output "registered", or driven, by flipflop) (col.10, ll.8-22; col.15, ll.20-47);

performing logic synthesis an each shell by utilizing a known delay for each wire (col.15, ll.58-67; col.45, ll.31-53; col.47, ll.26-38);

performing logic synthesis on each core (col.15, ll.58-67; col.45, ll.31-53; col.47, ll.26-38; col.70, ll.20-52); and

recombining (re-arranging) the cores and shells into blocks (loop for physical optimization) (col.45, ll.31-38; col.45, ll.54-67; col.46, ll.1-32).

As to claims 2-4, 9, 14 and 18-20 Dupenloup recites:

(2), (18) The method/program, wherein performing physical optimization of block placement comprises estimating an area of each block (col.79, ll.50-62);

(3), (19) The method/program, wherein performing physical optimization of wire placement comprises determining a pin (I/O) assignment layout (col.80, ll.13-17);

(4), (9), (14), (20) The method/program, wherein performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length ("routing by specifying the geometric information such as width of wires and their layers assignments") (col.80, ll.13-17).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-7, 10-12, 15-16 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dupenloup in view of Trimberger (US Patent 6,084,429).

4. With respect to claims 5-7, 10-12, 15-16 and 21-23 Dupenloup teaches the features above but lacks a method/computer readable media having stored instructions for synthesizing an integrated circuit design further comprising minimizing a delay in each wire by inserting buffers at optimal distances.

As to claims 5-7, 10-12, 15-16 and 21-23 Trimberger discloses:

(5)- (7), (10)-(12), (15)-(16), (21)-(23) The method, wherein performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances ("the buffering of the signal on a segmented

routing line may result in a faster signal path than if non-segmented lines,") (Abstract; col.1, ll.66-67; col.2, ll.1-12; col.2, ll.55-67; col.3, ll.1-9; col.4, ll.1-19).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Trimberger's teaching regarding the method/computer readable media having stored instructions for synthesizing an integrated circuit design further comprising minimizing a delay in each wire by inserting buffers at optimal distances and use it in Dupenloup's invention to ensure effective connectivity in the integrated circuit design, while substantially eliminating the longline capacitive-induced time delay by segmenting and buffering of the routing wires.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

Naum Levin
AU-2825